Abstract

Viterbi decoder

Viterbi decoder for decoding a received sequence of data symbols which are coded using a predetermined coding instruction, having:
(a) a branch metric calculation circuit (5) for calculation of branch metrics (λ) for the received sequence of coded data symbols;
(b) a path metric calculation circuit (9) for calculation of path metrics (γ) as a function of the branch metrics (λ) and the coding instruction,
with the calculated path metrics in each case being compared with an adjustable decision threshold value (SW) in order to produce an associated logic validity value; and having
(c) a selection circuit (20) which temporarily stores those path metrics whose validity value is logic high in a memory, and selects from the temporarily stored path metrics that path with the optimum path metric.

Figure 6